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Analysis of the electrical characteristics of *Zn/ZnSe/n-Si/Au–Sb* structure fabricated using SILAR method as a function of temperature

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ABSTRACT

The Successive Ionic Layer Adsorption and Reaction (SILAR) method has been used to deposit ZnSe thin film onto Si substrate to obtain the *Zn/ZnSe/n-Si/Au–Sb* sandwich structure. The X-Ray Diffraction (XRD) and Scanning Electron Microscope (SEM) methods are used to investigate the structural and morphological properties of films. The XRD and SEM studies reveal that the films are covered well on Si substrate and have good polycrystalline structure and crystalline levels. The current–voltage (*I–V*) and capacitance–voltage (*C–V*) characteristics of this structure have been investigated as a function of the temperature (80–300 K) with 20 K steps. The ideality factor (n) and zero-bias barrier height (Φ_{b0}) value which obtained from *I–V* curves were found to be strongly temperature dependent. While Φ_{b0} increases with increasing temperature, n decreases. This behavior of the Φ_{b0} and n can be attributed to barrier inhomogeneities at the metal–semiconductor (*M–S*) interface. The temperature dependence of the *I–V* characteristics of the *Zn/ZnSe/n-Si/Au–Sb* structure can reveal the existence of a double Gaussian distribution. The mean barrier height and the Richardson constant values are obtained as 0.925 eV and 1.140 eV, 130 A/cm^2 K^2 and 127 A/cm^2 K^2, from the modified Richardson plot, respectively. Furthermore, the barrier height and carrier concentration are calculated from reverse bias C^{-2}–V measurements at 200 kHz frequency as a function of the temperature.

1. Introduction

Metal–semiconductor (*M–S*) interfaces are an essential part of virtually all semiconductor electronic and optoelectronic devices. One of the most interesting properties of an *M–S* interface is its Schottky barrier height (*SBH*), which is a measure of the mismatch of the energy levels for majority carriers across the *M–S* interface. The *SBH* controls the electronic transport across *M–S* interfaces and is, therefore, of vital importance to the successful operation of any semiconductor device [1]. One of the most widely used techniques to measure the *SBH* is the *I–V* technique. Since, the current transport across the *M–S* interface is a temperature-activated process, analysis of the *I–V* characteristics of *M–S* contacts at room temperature does not only give detailed information about their conduction process or the nature of barrier formation at the *M–S* interface. The *I–V* measurements as a function of temperature are commonly used in the characterization of *M–S* interface [2]. The temperature dependence of the *I–V* characteristics allows to understanding different aspects of conduction mechanisms.

Since ZnSe is a valuable candidate in optoelectronic devices such as laser diodes, light-emitting diodes and photo detectors, there are currently a vast number of reports of experimental studies on ZnSe thin films [3–10]. Though a number of methods have been employed to synthesize ZnSe thin films [5], low luminescence efficiency caused by surface states is still a common problem for these films. The electrical and optical properties of ZnSe films are fairly sensitive to the structural properties of the films. Again the structural properties of thin film depend on the methods of preparation and deposition conditions. Up to now, various methods have been successfully developed to the syntheses of ZnSe thin films and their related physical and chemical properties. Chemical vapor deposition, metal–organic chemical vapor deposition, metal-catalyzed molecular beam epitaxy, and solution-based methods have been successfully applied in the synthesis of ZnSe thin films. Among these methods, SILAR is a relatively facile and inexpensive method. However, in the past there has been no report on preparation of sandwich structures by means of SILAR method. We report here how *Zn/ZnSe/n-Si/Au–Sb* structure has prepared and calculated of characteristics parameters of this structure. Being relatively easy, economical and suitable for large area deposition of any configuration, the SILAR method was reported in mid-1980s [11]. It does not require sophisticated instruments, and the substrate neither need to be conductive nor have a high melting point. The SILAR method is

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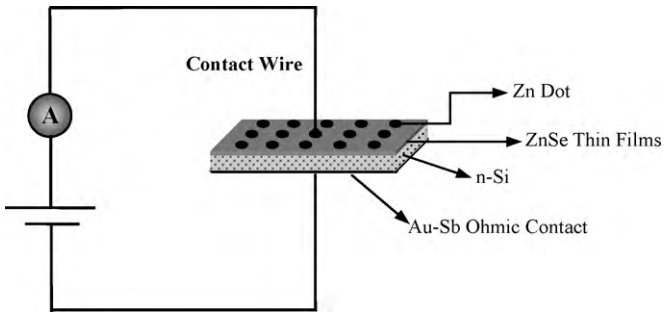

Fig. 1. The structure diagram of the fabricated device.

based on immersion of substrate into different cationic and anionic precursor solutions and rinsing before every immersion with highly purified deionized water to remove to loosely bounded species. The durations of adsorption, reaction and rinsing can be obtained experimentally. The growth of the film can be controlled at an accuracy of one SILAR deposition cycle [12,13].

In this work, the SILAR method was used to deposit the ZnSe thin film on n-Si substrate to obtain the *Zn/ZnSe/n-Si/Au–Sb* sandwich structure. The structural and morphological properties of ZnSe thin film were characterized using XRD and SEM methods. The *I–V* and *C–V* characteristics of this *Zn/ZnSe/n-Si/Au–Sb* structure were studied in wide temperature range by 20 K steps. It was seen that the barrier height inhomogeneties in this structure can be explained with the thermionic-emission mechanism with Gaussian distribution.

2. Experimental

We used cleaned and polished n-type Si semiconductor with (1 0 0) orientation and 1–10 Ω cm resistivity to fabricate the *Zn/ZnSe/n-Si/Au–Sb* sandwich structure (see Fig. 1). For the fabrication process, firstly Si wafer was dipped in boiling $NH_3 + H_2O_2 + 6H_2O$ solution for 10 min and then dipped in $HCl + H_2O_2 + 6H_2O$ at 60 °C for 10 min. Then, the wafer was dipped $HF + H_2O$ (1:10) solution and rinsed in deionized water with 18 MΩ to remove the native oxide layer on the front surface of the substrate. The wafer dried with high-purity nitrogen and inserted into the deposition chamber immediately. The Au–Sb alloy was evaporated onto the back side of wafer at vacuum pressure of 10^{-7} Torr. After evaporation of the alloy, in order to perform the ohmic contact, wafer annealed at 420 °C under N_2 atmosphere for 3 min. After ohmic contact was made, the ohmic contact side and the edges of the *n*-Si semiconductor substrate was covered by wax so that the polished and cleaned front side of the semiconductor sample was exposed to the cationic precursor solution employed for SILAR method. Zinc selenide thin films were deposited using $ZnCl_2$ and freshly prepared sodium selenosulphate (Na_2SeSO_3) solutions. The Na_2SeSO_3 solution was prepared by mixing 10 g selenium powder (99% purity) with 100 g anhydrous sodium sulphite (Na_2SO_3) in 500 ml of distilled water with constant stirring for 8–10 h at 80 °C. It was sealed and kept overnight, since on cooling, a little selenium separated out from the solution. It was then filtered to obtain a clear solution.

$ZnCl_2$ solution was used for cationic precursor. As a source of selenium ions, sodium selenosulphite was used. The growth parameters of ZnSe thin film are summarized in Table 1. The adsorption, reaction and rinsing times to growth ZnSe thin film were selected as 20 s, 30 s and 50 s, respectively. A single SILAR deposition cycle consisted of 20 s adsorption of Zn^{2+} ions, 50 s rinsing with double distilled water, 30 s adsorption and reaction of Se^{2-} ions with preadsorbed Zn^{2+} ions on the substrate and 50 s rinsing with double distilled water. By repeating such deposition cycles 45 times, we obtained homogeneous ZnSe thin films on Si substrate.

Table 1
Optimized growth parameters at room temperature (300 K) for the deposition of the ZnSe thin films.

Parameters	Precursors solutions	
	Zinc chloride	Sodium selenosulphate
Concentration (M)	0.1	0.13
pH	~5.5	~10.5
Immersion time	20	30
Rinsing time	50	50
Deposition cycles	45	45

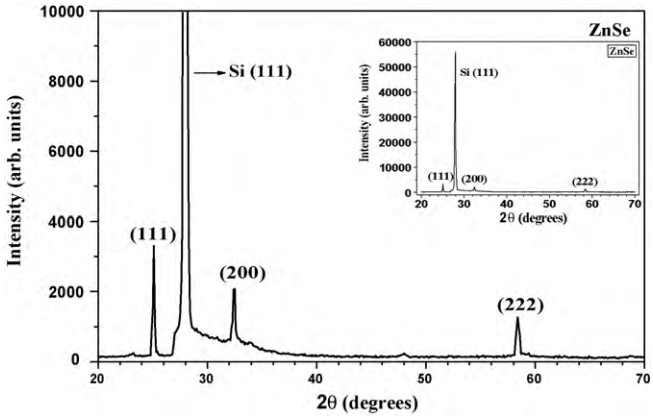

Fig. 2. The XRD patterns of ZnSe thin film.

The formation of ZnSe thin film involves following steps: in the anionic precursor solution, the hydrolysis of sodium selenosulphite releases selenide ions as,

$$Na_2SeSO_3 + OH^- \rightarrow Na_2SO_4 + HSe^-$$

$$HSe^- + OH^- \rightarrow H_2O + Se^{2-}$$

When the Si substrate is immersed in Zn^{2+} containing solution, Zn^{2+} ions are adsorbed on the surface of Si substrate. After immersion of such substrate in Se^{2-} ion containing solution, following reaction takes place,

$$Zn^{2+} + Se^{2-} \rightarrow ZnSe$$

For homogeneous thin film, these cycles have been repeated 45 times. The ZnSe layer thickness is defined as about 500 nm calculated from *C–V* measurement.

After this process, a homogeneous thin film layer has been formed over the substrate. Finally, the *Zn/ZnSe/n-Si/Au–Sb* structure was formed by evaporating Zn dots with diameter of 1.0 mm on the ZnSe thin film (the contact area = 7.85×10^{-3} cm^2). All evaporation processes were carried out in a vacuum coating unit. In this way, *Zn/ZnSe/n-Si/Au–Sb* sandwich structure was obtained. The structural and morphological properties of ZnSe thin films on Si substrate were characterized using XRD in the range of scanning angle 20–70° using Rigaku D/Max-IIIC diffractometer and ZEISS SUPRA 50VP SEM. The *I–V* and *C–V* measurements of the devices were made in the temperature range of 80–300 K using Leybold Heraeus closed-cycle helium cryostat, HP4140B picoammeter and a HP model 4192A LF impedance analyser under dark conditions.

3. Results and discussion

3.1. Structural and morphological properties of the ZnSe thin film

The structural analysis of ZnSe films was carried out using XRD with varying diffraction angle 2θ, from 20° to 70°. The XRD patterns of this film grown on Si substrate are shown in Fig. 2. As seen from the figure, zinc selenide can be grown with either hexagonal wurtzite type structure [Joint Committee of Powder Diffraction Standards (JCPDS) card no.: 15-105] or the cubic zincblende type structure [JCPDS card no.: 37-1463]. It is seen from the XRD patterns that the ZnSe films are in polycrystalline orientation along different planes and phases. The plane of Si(1 1 1) substrate is clearly observed in Fig. 2 and the plane intensity is dominant when compared with the others. The XRD patterns in Fig. 2 show well-resolved peaks d = 3.546 Å (1 1 1); d = 2.755 Å (2 0 0); d = 1.579 Å (2 2 2) and confirms that the formed compound is ZnSe thin film with cubic structure [19]. The observed d value is found to be 3.187 Å for single crystal Si(1 1 1) substrate. The value is agreed with standard d value taken from the JCPDS data files [14].

SEM is well-known technique to study the surface morphology of thin films. Fig. 3 shows SEM image of the ZnSe film. It is observed that the as-deposited ZnSe thin film is well covered the substrate without cracks or pinholes. Also, Fig. 3 shows that the surface morphology of the ZnSe thin film on the n-Si substrate is formed grains

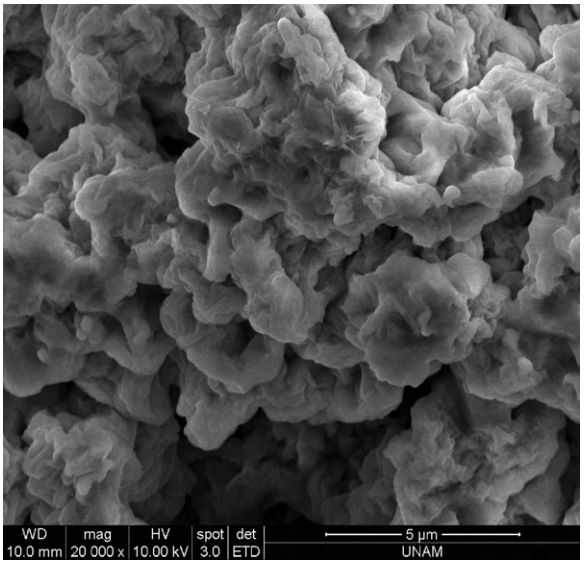

Fig. 3. SEM image of as-grown ZnSe thin film.

that have flower-like structure. The flower-like structures were observed on the entire film surface.

3.2. Temperature dependent I–V characteristics of Zn/ZnSe/n-Si/Au–Sb structure

Fig. 4 shows the semi-log forward and reverses bias *I–V* plots of the *Zn/ZnSe/n-Si/Au–Sb* structure in the temperature range of 80–300 K. For a *M–S* structure, it is assumed that the relationship between the applied forward bias and current of the device by the thermionic-emission theory given as follows [15,16],

$$I = I_0 \exp\left(\frac{eV}{nkT}\right)\left[1 - \exp\left(-\frac{eV}{kT}\right)\right] \quad (1)$$

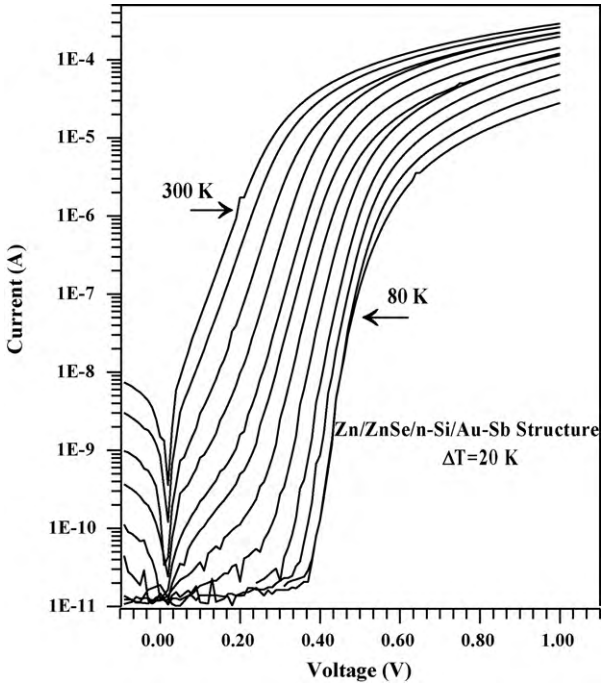

Fig. 4. The semi-log reverse and forward bias current–voltage characteristics of *Zn/ZnSe/n-Si/Au–Sb* sandwich structure at various temperatures.

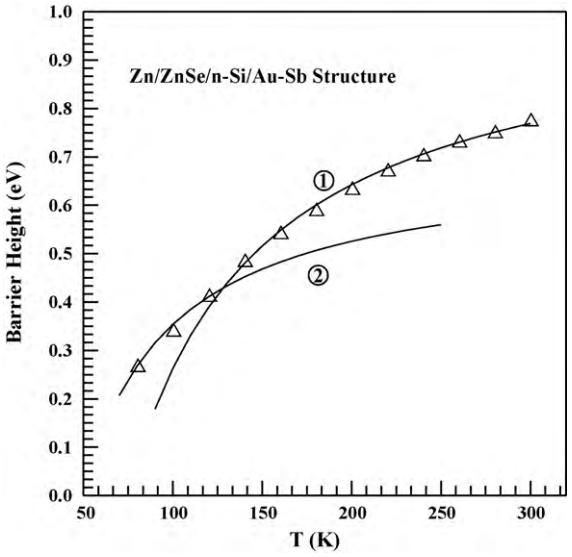

Fig. 5. Temperature dependence of barrier height for *Zn/ZnSe/n-Si/Au–Sb* structure. The continuous curves represent estimated values of Φ_{ap} using Eq. (9) for two Gaussian distributions of barrier heights with $\overline{\Phi}_b = 0.756$ eV and $\sigma_s = 68.00$ mV in 130–300 K (the curve 2) and $\overline{\Phi}_b = 1.021$ eV and $\sigma_s = 130.06$ mV in 80–130 K (the curve 1).

where n is the ideality factor, k is the Boltzmann constant, e is the electron charge, V is the forward bias voltage, T is the absolute temperature and I_0 is the saturation current and is given by

$$I_0 = AA * T^2 \exp\left(-\frac{e\Phi_b}{kT}\right) \quad (2)$$

A^*, A, Φ_{b0} are the effective Richardson constant of 112 A/cm^2 K^2 for n-type Si, the area of the rectifier contact, the experimental zero-bias *BH*, respectively. The value of ideality factor n can be obtained from Eq. (1) as follows,

$$n = \frac{e}{kT}\frac{dV}{d(\ln I)} \quad (3)$$

The values of ideality factor and barrier height have been obtained from intercept and slope of the linear portion of the forward bias ln(I)–V plots at each temperatures. The experimental values of Φ_{b0} and n for the *Zn/ZnSe/n-Si/Au–Sb* structure were ranged from 0.779 eV and 1.217 (at 300 K) to 0.271 eV and 4.955 (at 80 K), respectively. The ideality factor n is a measure of conformity of the diode to pure thermionic emission. Temperature dependence of ideality factor shows that the forward bias transport properties of the present device are not well modeled by the thermionic emission only. This suggests that the current processes occurring in the highly resistive ZnSe layer of the *Zn/ZnSe/n-Si/Au–Sb* structure would be a possible alternative candidate in determining the forward current. The barrier height values decreased and n values increased with decreasing temperature. The high value of n can be attributed to the effects of the bias voltage drop across the interfacial layer, particular distribution of the interface states at the semiconductor interface and the special barrier inhomogeneties at the metal–semiconductor interface [16–19].

Because of temperature-activated process, the current transport is dominated by current flowing through the lower *SBH* and a large ideality factor [20]. In other words, as the temperature increases, more and more electrons have sufficient energy to surmount the higher barrier. As a result, the dominant Φ_{b0} increases with increasing temperature and bias voltage. The values of the barrier height versus temperature are shown in Fig. 5. The barrier height values also exhibit strong temperature dependence.

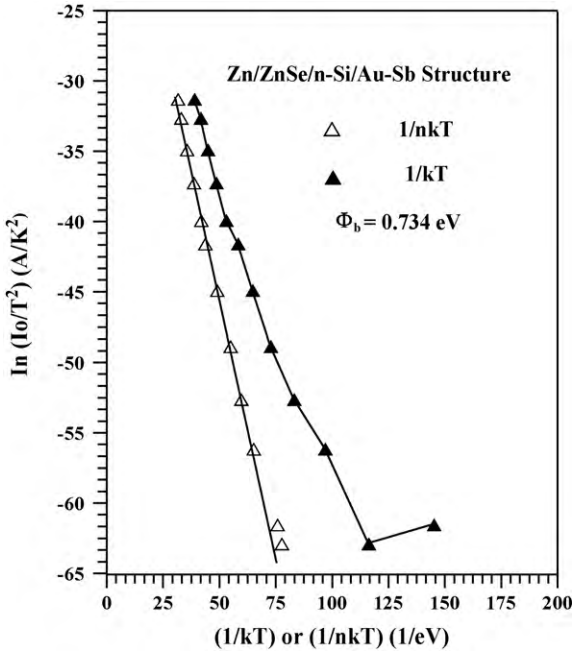

Fig. 6. Richardson plots of the $\ln(I_0/T^2)$ versus $1/T$ (the closed triangles) and $\ln(I_0/T^2)$ versus $1/nT$ (the open triangles) for *Zn/ZnSe/n-Si/Au–Sb* structure.

For the another evaluation of *BH*, Eq. (2) can be rewritten as

$$\ln\left(\frac{I_0}{T^2}\right) = \ln(AA^*) - \frac{e\Phi_b}{kT} \tag{4}$$

Fig. 6 shows the $\ln(I_0/T^2)$ versus $1/kT$ and $1/nkT$. The slope of activation energy $\ln(I_0/T^2)$ versus $1/kT$ plot allows us the determination of the effective *BH*. This plot is indicated by the closed triangles in Fig. 6. The deviation in the experimental $\ln(I_0/T^2)$ versus $1/kT$ curve at low temperatures can be explained by the temperature depended of the *BH* and ideality factor due to the presence of the spatially inhomogeneous *BH* and potential [1,21–34]. The current through the diode flows preferentially through the lower barriers in the potential distribution. Likewise, the activation energy $\ln(I_0/T^2)$ versus $1/nkT$ plot (open triangles) with the ideality factors was drawn and this plot yielded a 0.734 eV value for effective *BH*.

In order to describe barrier inhomogenity, different types of barrier distribution function at the interface have been reported [15,16]. We use the model of Werner and Güttler, introducing a Gaussian distribution (*GD*) in *BH*s with a mean value Φ_{b0} and Standard deviation σ_s in the form.

$$P(\Phi_b) = \frac{1}{\sigma_s\sqrt{2\pi}} \exp\left(-\frac{\left(\Phi_b - \bar{\Phi}_b\right)^2}{2\sigma_s^2}\right) \tag{5}$$

where $1/\sigma_s\sqrt{2\pi}$ is the normalization constant of *GD* of the barrier height. The total current $I(V)$ across the Schottky barrier diode at a forward bias can be expressed as

$$I(V) = \int_{-\infty}^{+\infty} I(\Phi_b, V)P(\Phi_b)d\Phi_b \tag{6}$$

where $I(\Phi_b,V)$ is the current based on the ideal thermionic-emission model and $P(\Phi_b)$ is the normalized distribution function giving the probability of accuracy for the barrier height. Now, introducing $I(\Phi_b,V)$ and $P(\Phi_b)$ from Eqs. (1) and (5) into Eq. (6), and performing integration from $-\infty$ to $+\infty$, one can obtain the current $I(V)$ through a barrier at a forward bias V, similar to Eqs. (1) and (2) but with the modified barrier [15,16,35].

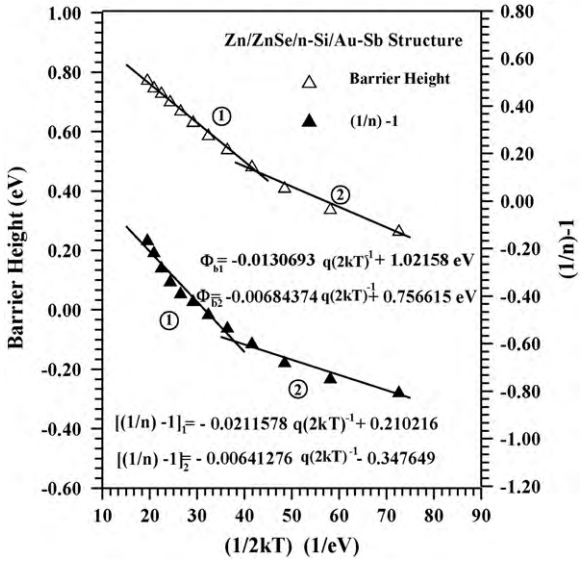

Fig. 7. Zero-bias apparent barrier height (the closed triangles) and ideality factor (opentriangles) versus $1/(2kT)$ curves of the *Zn/ZnSe/n-Si/Au–Sb* structure according to two Gaussian distributions of barrier heights.

$$I(V) = AA * T^2 \exp\left[-\frac{e}{kT}\left(\overline{\Phi}_b - \frac{e\sigma_s^2}{2kT}\right)\right] \exp\left(\frac{eV}{n_{ap}kT}\right) \left[1 - \exp\left(-\frac{eV}{kT}\right)\right] \tag{7}$$

with

$$I_0 = AA * T^2 \exp\left(-\frac{e\Phi_{ap}}{kT}\right) \tag{8}$$

where Φ_{ap} and n_{ap} are the apparent *BH* and ideality factor, respectively, and are given by

$$\Phi_{ap} = \overline{\Phi}_b - \frac{e\sigma_s^2}{2kT} \tag{9}$$

$$\left(\frac{1}{n_{ap}} - 1\right) = -\rho_2 + \frac{e\rho_3}{2kT} \tag{10}$$

It is assumed that the modified *SBH*, $\overline{\Phi}_b$ and σ_s are linearity bias dependent on Gaussian parameters, such as $\overline{\Phi}_b = \overline{\Phi}_{b0} + \rho_2 V$ and standard deviation $\sigma_s = \rho_{s0} + \rho_3 V$, where ρ_2 and ρ_3 are voltage coefficients that may depend on T. The temperature dependence of σ_s is usually small and can be neglected [1,15,35].

The experimental Φ_{ap} versus $1/T$ and n_{ap} versus $1/T$ plots were drawn by means of experimental data obtained from Fig. 7 respond to two lines instead of single line with transition occurring at 130 K. The above observations indicate the presence of two Gaussian distributions of barrier height in the contact area. The linearity of the apparent *BH* versus $1/T$ curves in Fig. 7, and the continuous curve in Fig. 5 show that the temperature dependent experimental data of the *Zn/ZnSe/n-Si/Au–Sb* sandwich structure are in agreement with the recent model which is related to thermionic emission over a Gaussian *BH* distribution [36–43].

The ideality factor depended of the temperature is seen Eq. (10). The plot of n_{ap} versus $1/T$ should be straight line that gives voltage coefficients ρ_2 and ρ_3 from the intercept and slope respectively. The values of $\rho_2$were obtained 0.347 in 130–300 K and 0.210 in 80–130 K temperature ranges. The plot of Φ_{ap} versus $1/T$ should be a straight line that gives $\overline{\Phi}_b$ and σ_0 from the intercept and slope, respectively. The values of $\overline{\Phi}_{b0}$ and σ_0 are 0.756 eV and 68 mV

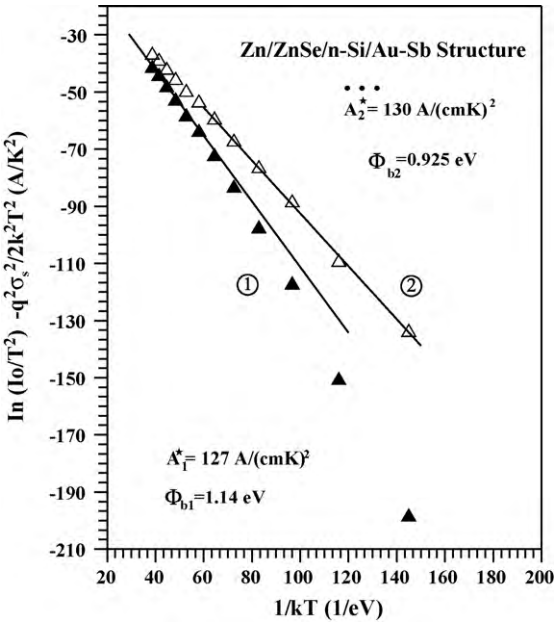

Fig. 8. Modified Richardson $\ln(I_0/T^2) - (q^2\sigma_s^2/2k^2T^2)$ versus $1/T$ plots for the *Zn/ZnSe/n-Si/Au–Sb* structure according to two Gaussian distributions of barrier heights.

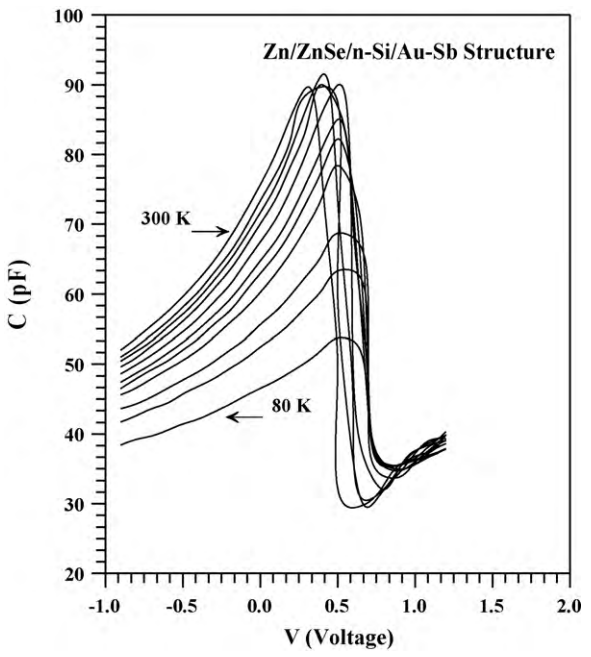

Fig. 9. Experimental reverse and forward bias *C–V* characteristics of *Zn/ZnSe/n-Si/Au–Sb* sandwich structure at various temperatures.

in 80–130 K temperature range and as 1.021 eV and 130 mV in 130–300 K temperature range. In addition, the experimental Φ_{ap} values are in agreement with the theoretical values obtained using Eq. (8). The continuous solid line in Fig. 5 represents these theoretical values. According to the these results, the non-ideality in the *M–S* contacts is due to the inhomogeneity that is caused by non-uniformity of the interfacial charges, grain boundaries, multiple phases, facets, a mixture of different phases, etc. [1,15,36].

The Richardson plot is modified by combining Eqs. (8) and (9)

$$\ln\left(\frac{I_0}{T^2}\right) - \left(\frac{e^2\sigma_s^2}{2kT^2}\right) = \ln(AA^*) - \frac{e\overline{\Phi}_b}{kT} \tag{11}$$

Using the experimental I_0 data, a modified $\ln(I_0/T^2) - (e^2\sigma_s^2/2k^2T^2)$ versus *1/T* plot according to Eq. (11) should give a straight line with the slope directly yielding the mean barrier height and the intercept ($\ln AA^*$) at the ordinate determining A^* for a given diode area *A*. The $\ln(I_0/T^2) - (e^2\sigma_s^2/2k^2T^2)$ values were calculated using two values of σ_s obtained for the two temperature ranges of 80–130 K and 130–300 K. The modified $\ln(I_0/T^2) - (e^2\sigma_s^2/2k^2T^2)$ versus *1/T* plots for the two values of σ_s have been given in Fig. 8 as closed and open triangles. The best linear fit to these modified experimental data is depicted by solid lines in Fig. 8 which represent the true activation energy plots in two temperature ranges. The calculations yielded zero-bias mean barrier height Φ_{b0} is 0.925 eV (in the range of 80–130 K) and 1.140 eV (in the range of 130–300 K). This value of Φ_{b0} is approximately accommodating the values of Φ_{b0} obtained from the plot of Φ_{ap} versus *1/T* give Fig. 7. The intercepts at the ordinate give the Richardson constant A^* as 130 A/cm^{2}K^2 (in 80–130 K range) and 127 A/cm^{2}K^2 (in 130–300 K) without using the temperature coefficient of the *BH*s. While modified Richardson constants $A_1^* = 127$ A/cm^2 K^2, $A_2^* = 130$ A/cm^2 K^2 is in agreement with the known value of $A^* = 112$ A/cm^2 K^2 for n-Si.

3.3. Temperature dependent C–V characteristics of Zn/ZnSe/n-Si/Au–Sb structure

It is convenient to examine *C–V* data of the devices by plotting C^{-2}–*V* under reverse bias. In metal–semiconductor structure, the depletion layer capacitance, *C* can be expressed as [15]

$$C^{-2} = \frac{2(V_d + V)}{\varepsilon_s\varepsilon_0 eA^2N_d} \tag{12}$$

where *A* is the area of the contact, V_d is the diffusion potential at zero-bias and is determined from the extrapolation of the linear C^{-2}–*V* plot to the *V* axis, ε_s is the dielectric constant of the semiconductor, N_d is the donor concentration of n-type semiconductor substrate. With help of Eq. (12), the values of V_d and N_d can be determined from the intercept and slope of the C^{-2}–V plot, respectively.

The value of the *BH* can be calculated by $\Phi_b = V_d + V_n$ equation using *C–V* data, where V_n is the potential difference between the Fermi energy level (E_f) and the bottom of the conduction band in the neutral region of *n*-Si, which is directly equal to E_f and can be calculated by knowing N_d and N_c, density of states in the conduction band ($N_d = N_c \exp(V_n/kT)$). Measurement of the depletion region capacitance under forward bias is difficult because the diode is conducting and the capacitance is shunted by a large conductance. However, the capacitance can be easily measured as a function of the reverse bias. Figs. 9 and 10 show *C–V* and reverse bias C^{-2}–*V* characteristics of *Zn/ZnSe/n-Si/Au–Sb* structure in the temperature range of 80–300 K at 200 kHz frequency, respectively. As can be seen from the figures, the capacitance values increase at high temperatures. This observation may be attributed to the increase of mobile charges with increasing sample temperature. Also, it can be seen from the reverse bias C^{-2}–*V* figure that these curves are linear. This indicates that the formation of this structure resembles a Schottky diode and allows the use of the simple depletion layer theory. The barrier height and the carrier concentration were calculated in the reverse bias C^{-2}–*V* characteristics in Fig. 10. Fig. 11 shows Φ_{c-v} (indicated by open triangles) values obtained from the reverse bias C^{-2}–*V* characteristics depending on temperature. The experimental Φ_{c-v} versus *T* plot yields Φ_{c-v} ($T = 0$) = 1.754 eV and $\alpha = -0.00268$ mev/K, where α is the temperature coefficient of the *BH*. The *BH* extracted from the *C–V* measurements increases quickly with decreasing temperature, in contrast to the *I–V* measurements. Therefore, there is more current at low temperature than predicted by thermionic-emission theory and the results of

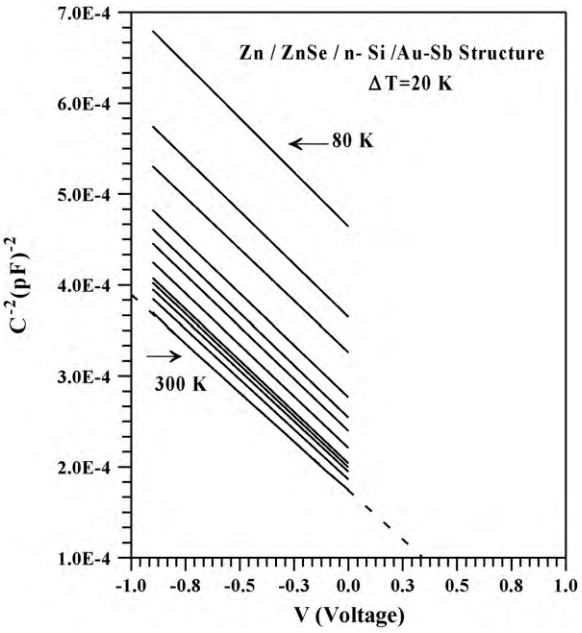

Fig. 10. Experimental reverse bias C^{-2}–V characteristics of *Zn/ZnSe/n-Si/Au–Sb* sandwich structure at various temperatures.

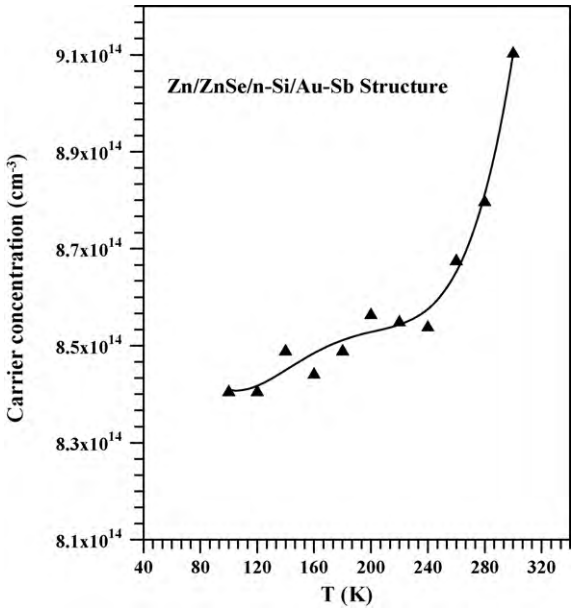

Fig. 12. Temperature dependence of the carrier concentration obtained from experimental reverse bias C^{-2}–V characteristics of *Zn/ZnSe/n-Si/Au–Sb* sandwich structure.

the C–V measurements. Fig. 12 shows the temperature dependence of the experimental carrier concentration was calculated from the reverse bias C^{-2}–V characteristics. As can be seen Fig. 12, carrier concentration of the *Zn/ZnSe/n-Si/Au–Sb* structure slightly decreased with decreasing in temperature within the 80–240 K temperature range. On the other hand, in 240–300 K temperature range, the decreasing is higher.

It is seen that the barrier height obtained from I–V measurement is always smaller than the average of the barrier height obtained from C–V measurements. Some general causes for these differences in barrier height have been mentioned in the literature, such as surface contamination at the interface, deep impurity levels, an intervening insulating layer, quantum mechanical tunneling, image force lowering and edge leakage currents [1,16,37]. In addition, there are many reports showing the discrepancy between *BH*s measured by different techniques might be associated with instrumentation problems; namely, how to determine the true space-charge capacitance from C–V data, or a large series resistance, which could affect the value determined by I–V measurements [1]. If the barriers are uniform and ideal, the two measurements yield the same value; otherwise they will yield different values.

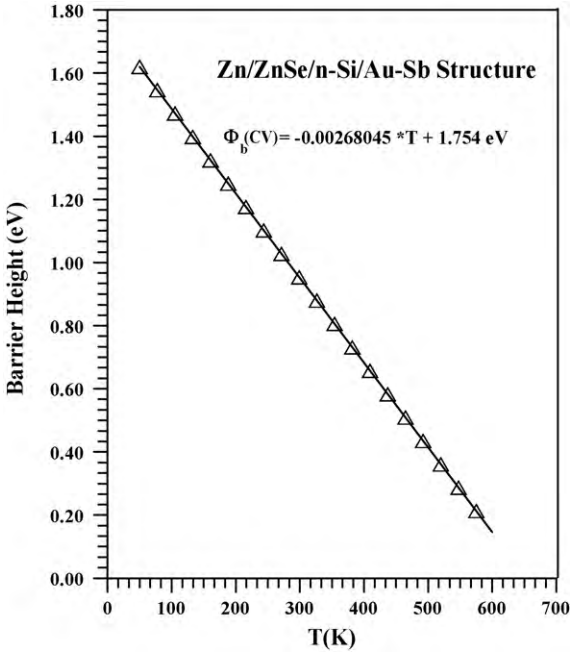

Fig. 11. Temperature dependence of the barrier height obtained from experimental reverse bias C^{-2}–V characteristics of *Zn/ZnSe/n-Si/Au–Sb* sandwich structure.

4. Conclusions

In this study, SILAR method has been used first time to deposit ZnSe film on Si substrate. The XRD and SEM methods are used for investigation of structural and morphological properties of films. The XRD and SEM studies reveal that the films are covered well with Si substrate and exhibit polycrystalline characterization. The I–V and C–V characteristics of *Zn/ZnSe/n-Si/Au–Sb* structure have been investigated as a function of the temperature in the temperature range (80–300 K). The ideality factor (n) and zero-bias barrier height (Φ_{b0}) values which obtained from I–V curves were found to be strongly temperature dependent. While *BH* increases, n decreases with increasing temperature. The electrical measurements of the *Zn/ZnSe/n-Si/Au–Sb* structures demonstrate that temperature dependence explained on the basis of the thermionic emission with Gaussian distribution of the barrier height. The activation energy $\ln(I_0/T^2)$ versus $1/nkT$ plot yielded a straight line with on effective *BH* of value 0.734 eV. The double *GD* has mean barrier height (Φ_{b0}) of 0.756 eV and 1.021 eV and standard deviations (σ_s) of 0.006 V and 0.013 V, respectively. These values match exactly with the mean *BH*s obtained from Φ_{ap} versus $1/T$ plot. The values of Φ_{b0} and Richardson constants (A^*) are obtained from a modified $\ln(I_0/T^2) - (q^2\sigma_s^2/2k^2T^2)$ versus $1/T$ plot as 0.925 eV and 1.140 eV and 130 A/cm^2 K^2 and 127 A/cm^2 K^2, respectively. These values of Richardson constants are in a very close agreement with to the theoretical value of 112 A/cm^2 K^2 for n-Si.

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